- Wide Input Voltage Range: 2.7V-12V
- [illegible]

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

ILIM	8

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

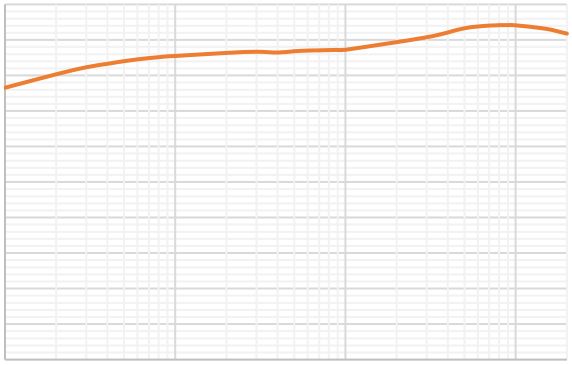


Figure 1. SCT1271 Efficiency vs Load Current, Vout=9V

Figure 2. SCT1271 Efficiency vs Load Current, Vin=3.6V

Figure 3. Load Regulation (Vin=3.6V, Vout=9V)

Figure 4. Line Regulation, Vout=9V

Figure 5. Current Limit VS Setting Resistance

Figure 6. Switching Frequency VS Setting Resistance

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

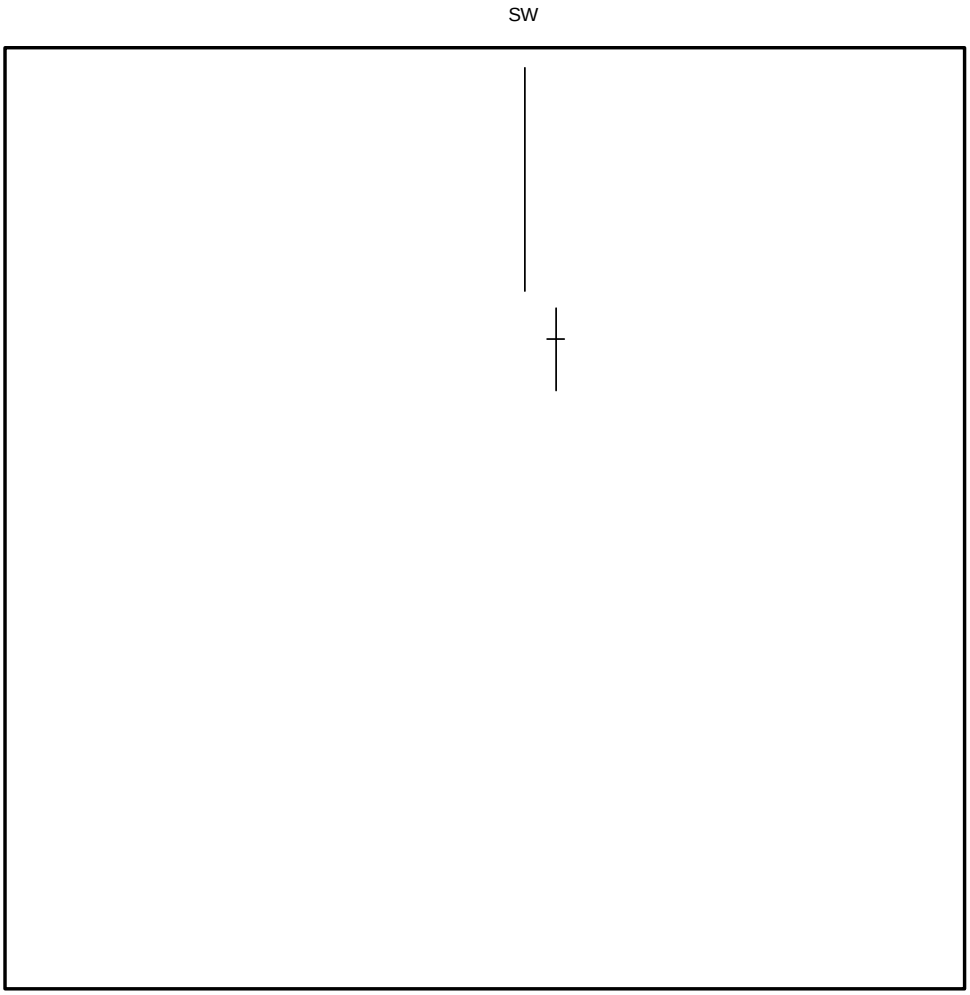


Figure 7. Functional Block Diagram

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

(minimum 0.4V). An internal 750KΩ resistor connects EN pin to the ground. Floating EN pin automatically disables the device.

The SCT1271 features fixed 4ms soft start to prevent inrush current during power-up.

Adjustable Peak Current Limit

The SCT1271 boost converter implements cycle-by-cycle peak current limit function with sensing the internal low-side power MOSFET Q1 during overcurrent condition. While the Q1 is turned on, its conduction current is monitored by the internal sensing circuitry. Once the low-side MOSFET Q1 current exceeds the limit, it turns off immediately. An external resistor connecting ILIM pin to ground sets the low-side MO1 peak current limit threshold. Use /MCIquation1 or Figure 5 to calculate the peak current limit.

(1)

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance between ILIM pin to grnd.

This current limit function is realized by detecting the current flowing through the low-side MOSFET. The current limit feature loses function in the output hard short circuit conditions. At normal operation, when the output hard shorts to ground, there is a direct path to short the input voltage through high-side MOSFET Q2 or its body diode even the Q2 is turned off. This could damage the circuit components and cause catastrophic failure at load circuit.

Adjustable Switching 77/LFrequency

The SCT1271 features a wide adjustable switching frequency ranging from 200kHz to 2.2MHz. The switching frequency is set by a resistor connected between the FSW pin and the GND pin of SCT1271. Do not leave the W pin open. Use /MCIquation2 to calculate the resistor value required for a desired frequency.

(2)

where:

- f_{SW} is the desired switching frequency
- T_{DELA} [redacted] ns
- C_{FREQ} = 6 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Over Voltage Protection 77/Lan 77/d Min 7-Time um On

The SCT1271 features VOUT pin over voltage protection. If the VOUT pin is above 13.2V typical, the device stops switching immediately until the VOUT pin drops below 12.92V.F3 9.96 Tf1 0 0 1 53831 275.81 257.45 Tm0 g0 G[ )]TJETQ EM

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

and reaches a threshold with respect to the peak current of I_{LIM} / 10, the output of the error amplifier is clamped at this value and does not decrease any more. If the load current is smaller than what the SCT1271 delivers, the output voltage increases above the nominal setting output voltage. The SCT1271 extends its off time of the switching period to deliver less energy to the output and regulate the output voltage to 1.0% higher than the nominal setting voltage. With the PFM operation mode, the SCT1271

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Typical Application

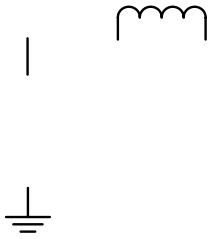


Figure 8. One Cell Battery Input, 9V/2A (20W) Output

Design Parameters

Design Parameters	Example Value
Input Voltage	3.0V to 4.35V
Output Voltage	9V
Output Current	2A
Output voltage ripple (peak to peak)	100mV
Switching Frequency	500 kHz
Operation Mode	PFM

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Switching Frequency

The resistor connected from FSW to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation 3. High frequency can reduce the inductor and output capacitor size with the tradeoff of more thermal dissipation and lower efficiency.

(3)

where:

- f_{SW} is the desired switching frequency
- T_{DELAY} = 70 ns
- C_{FREQ} = 6 pF
- V_{IN} is the input voltage
- V_{OUT} is the output voltage

Fsw	R_{FREQ}
200 KHz	1240 KΩ
370 KHz	523 KΩ
560 KHz	309 KΩ
860 KHz	180 KΩ
1000 KHz	150 KΩ
2000 KHz	57 KΩ

Peak Current Limit

Using the correct external resistor at ILIM pin sets the peak input current. Table 2 shows the resistor value for inductor peak current limit. For a typical current limit of 9.5A, the resistor value is 84KΩ. The minimum current limit must be higher than the required peak switch current at lowest input voltage and the highest output power not to hit the current limit and still regulate the output voltage.

(4)

where:

- I_{LIM} is the peak current limit
- R_{LIM} is the resistance of ILIM pin to ground

I_{LIM}	R_{LIM}
9.5 A	84 KΩ
8 A	100 KΩ
5.6A	142 KΩ
4A	200 KΩ

Output Voltage

The output voltage is set by an external resistor divider R3 and R4 in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of R3 can be calculated by equation 5.

(5)

where:

- V_{REF} is the feedback referenceQ EM(e)-9(ferenc)-3(eQ EM(e81((.)]TJETQ, EMC /Span &MCID 154/Lang (en-US)2

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Inductor Selection

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

calculations and bench evaluation. In this application, the Wurth-Elektronix 's inductor 744313220 is used on SCT1271 evaluation board.

Table 4. Recommended Inductors

Part Number	L (uH)	DCR Max (mΩ)	Saturation Current/Heat Rating Current (A)	Size Max (LxWxH mm)	Vendor
744325180	1.8	3.5	18 / 14	10.5 x 10.2 x 4.7	Wurth Elektronix
744311150	1.5	7.2	14 / 11	7.3 x 7.2 x 4.0	Wurth Elektronix
744311220	2.2	12.5	13 / 9	7.3 x 7.2 x 4.0	Wurth Elektronix
744313220	2.2	5.7	18 / 14	12.9 x 12.8 x 3.3	Wurth Elektronix
CDMC8D28NP-1R8MC	1.8	12.6	9.4 / 9.3	9.5 x 8.7 x 3.0	Sumida

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT1271. A ceramic capacitor of more than 1.0μF is required at the VCC pin to get a stable operation of the internal LDO.

For the power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, 2x 22μF input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, three 22μF ceramic output capacitors work for most applications. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation 9 and 10 to calculate the minimum required effective capacitance, C_{OUT}.

(9)

(10)

where

- V_{ripple_C} is output voltage ripple caused by charging and discharging of the output capacitor.
- V_{ripple_ESR} is output voltage ripple caused by ESR of the output capacitor.
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- I_{Lpeak} is the peak current of the inductor.
- f_{SW} is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Loop Stability

An external loop compensation network comprises resister R5, ceramic capacitors C5 and C6 connected to the COMP pin to optimize the loop response of the converter. The power stage small signal loop response of constant off time with peak current control can be modeled by equation 11.

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

(18)

If the calculated value of C6 is less than 10pF, it can be left open. Designing the loop for greater than 45°of phase margin and greater than 10-dB gain margin eliminates output voltage ringing during the line and load transient.

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms

Vin=3.6V, Vout=9V, unless otherwise noted

Figure 9. Power up

Figure 10. Power down

Figure 11. EN Power up (Iload=2A)

Figure 12. EN Power down(2A)

Figure 13. EN toggle (Iload=2A)

Figure 14. EN toggle (Iload=10mA)

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Application Waveforms(continued)

Vin=3.6V, Vout=9V, unless otherwise noted

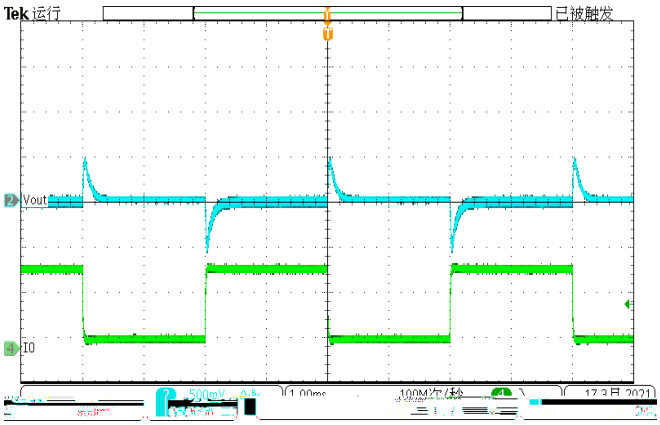


Figure 15. Load transient (0.2A-1.8A, 1.6A/us)

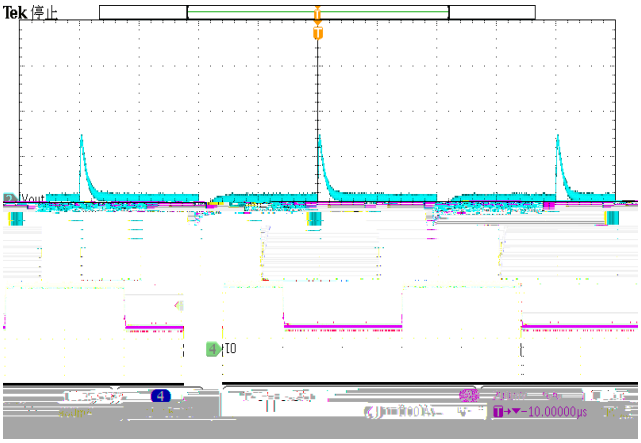


Figure 16. Load transient (0.5A-1.25A, 1.6A/us)

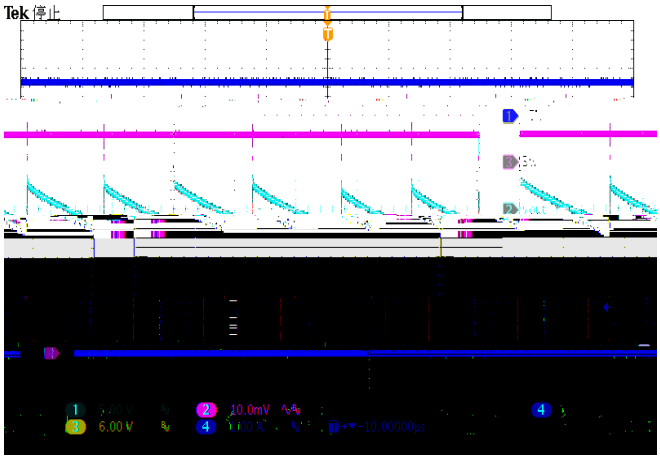


Figure 17. Steady state (Iload=0A, PFM)

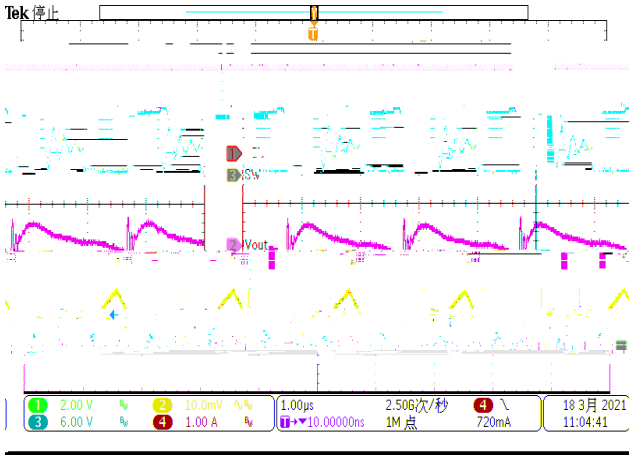


Figure 18. Steady state (Iload=150mA, PFM)

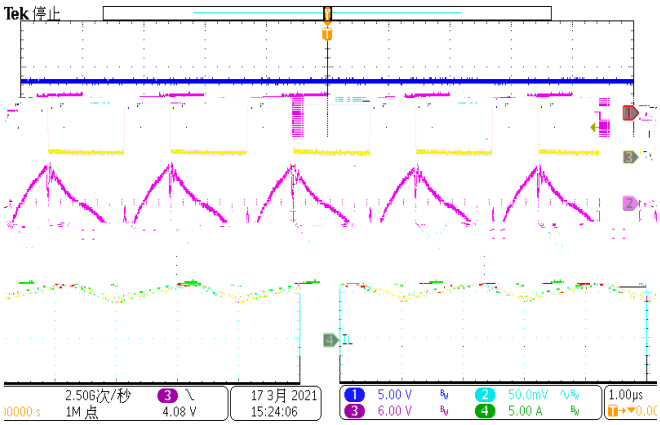


Figure 19. Steady state (Iload=2A)

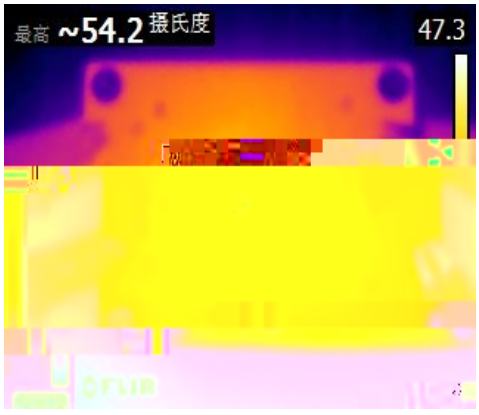


Figure 20. Thermal, Vin=3.6V, Vout=9V, Iload=2A

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Layout Guideline

The regulator could suffer from instability and noise problems without careful layout of PCB. Radiation of high-frequency noise induces EMI, so proper layout of the high-frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin, and always use a ground plane under the switching regulator to minimize coupling. The input capacitor needs to be close to the VIN pin and ground pad to reduce the input supply ripple.

The most critical current path for all boost converters is from the switching FET, through the rectifier FET, then the output capacitors, and back to ground of the switching FET. This high current path contains nanosecond rise time and fall time, and should be kept as short as possible. Therefore, the output capacitor needs not only to be close to the VOUT pin, but also to the GND pin to reduce the overshoot at the SW pin and VOUT pin. The placement and ground trace for

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

Thermal Considerations

The maximum IC junction temperature should be restricted to 150℃ under normal operating conditions. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual power dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using Equation 19.

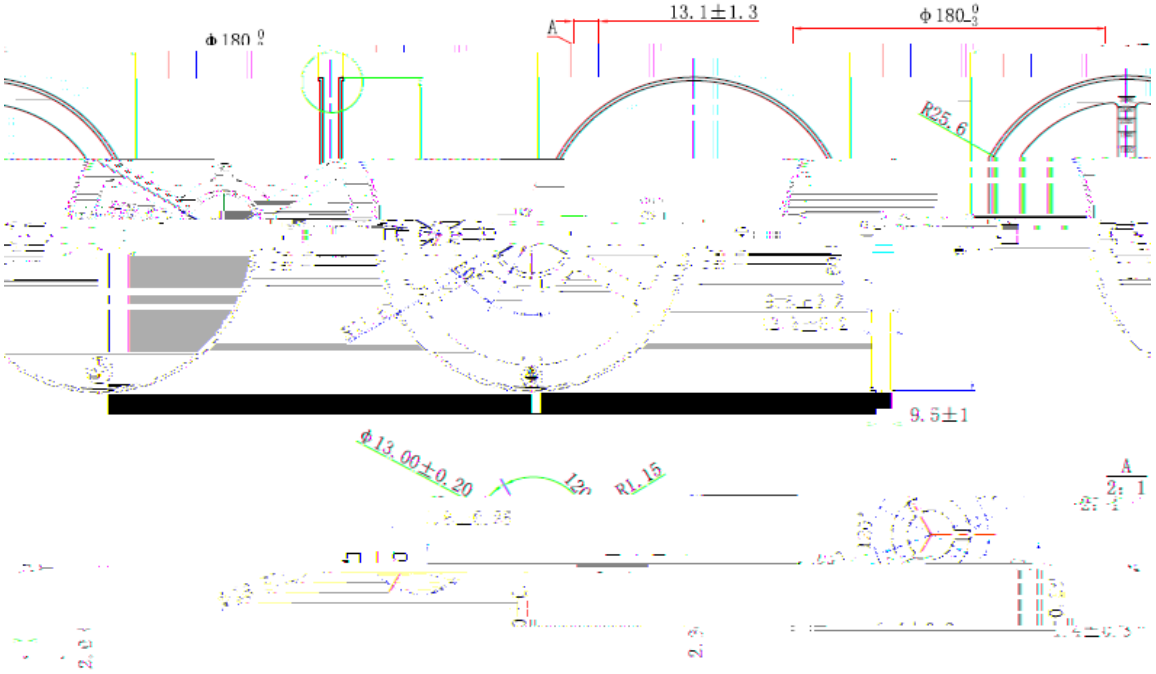
(19)

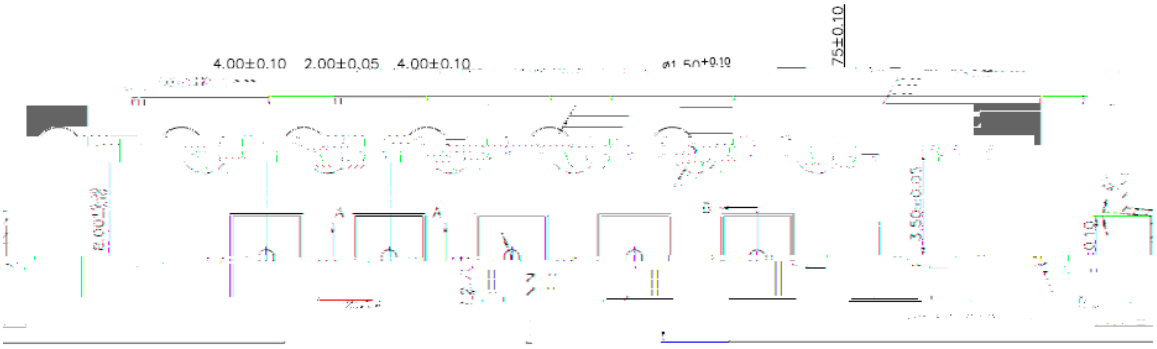
where

- T_A is the maximum ambient temperature for the application.
- $R_{\theta JA}$

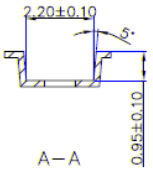
 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved

 © 2025 Silicon Content Technology Co., Ltd.





B–B



A–A

 © 2025 Silicon Content Technology Co., Ltd. All Rights Reserved