Up to 28V Supply, 4-A Dual Channel High Speed Low Side Driver

FEATURES

- Wide Supply Voltage Range: 4.5V - 28V
- 4A Peak Source Current and 4A Peak Sink Current
- Stackable Output for Higher Driving Capability
- Negative Input Voltage Capability: Down to -5V
- TTL Compatible Input Logic Threshold
- Propagation Delay: 13ns
- Typical Rising and Falling Times: 8ns
- Typical Delay Matching: 1ns
- Low Quiescent Current: 55
- Output Low When Input Floating
- Independent Enable Logic for Each Channel
- Thermal Shutdown Protection: 170℃
- Available in SOP-8 and eMSOP-8 Package

APPLICATIONS

- IGBT/MOSFET Gate Driver
- Variable Frequency-Drive (VFD)
- Switching Power Supply
- Motor Control
- Solar Power Inverter

DESCRIPTION

The SCT52240a is a wide supply, dual channel, high speed, low side gate drivers for both power MOSFET IGBT. Each channel can source and sink 4A peak current alon with rail- -rail output capability. The 28 power supply rail enhances the driver output ringing endurance during the power device transition.

The minimum 13ns input to output propagation delay enables the SCT52240A suitable for high frequency power converter application.

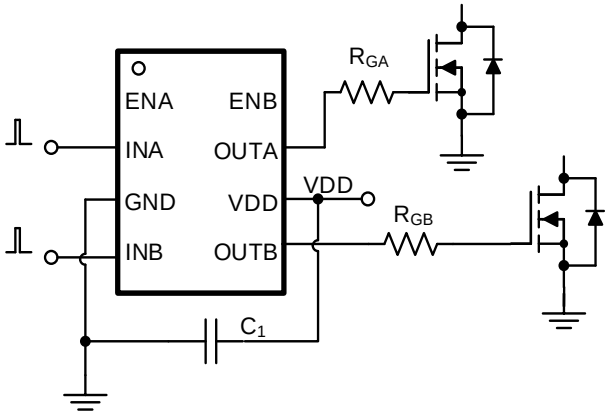
The SCT52240A features wide input hysteresis that is compatible for low voltage logic. The SCT52240a has the capability to handle negative input down to -5V, which increases the input noise immunity.

The SCT52240A has very low quiescent current that reduces the stand-by loss in the power converter. The SCT52240A each channel driver adopts non-overlap driver design to avoid the shoot-through of output stage. The two channels INA and INB have critical propagation delay matching and artificial dead time implemented in output stage, which enable stackable output available when the system needs higher driving capability.

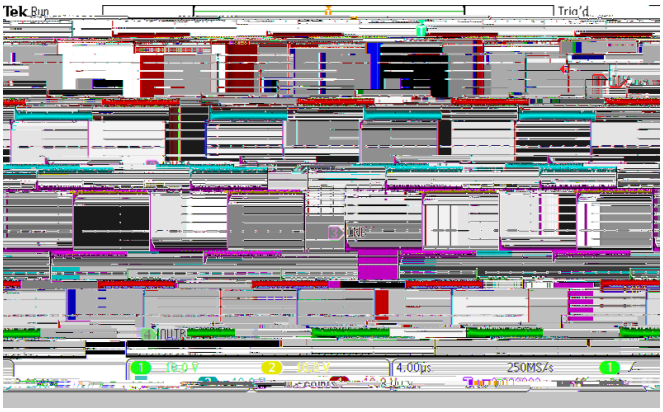
The SCT52240A features 170℃ thermal shut down. The SCT52240a is available in SOP-8 and eMSOP-8 ckage.

TYPICAL APPLICATION

SCT52240a Typical Application



Application Waveform



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eserved

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{DD}	Supply voltage range	4.5	28	V
$V_{INA,INB}$	Input voltage range	-5	24	
T_J	Operating junction temperature	-40	125	℃

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TYPICAL CHARACTERISTICS

V_{IN}=12V, T_A= 25℃.

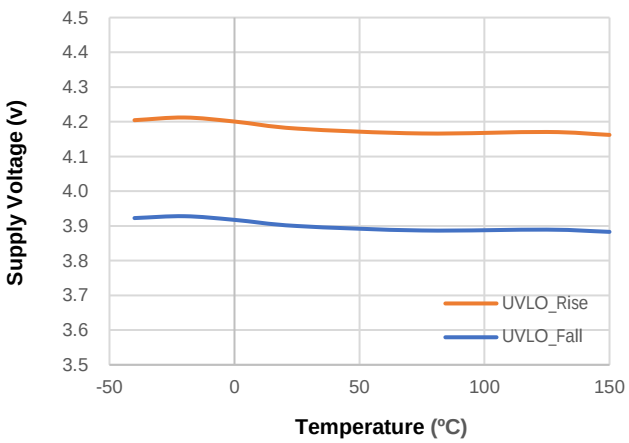

Figure 1. UVLO vs Temperature

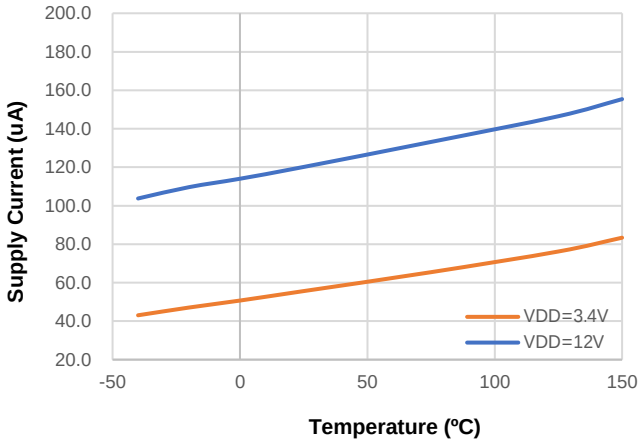

Figure 2. Supply current vs Temperature

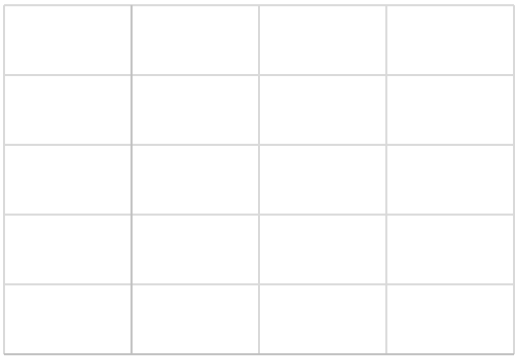

Figure 3. Input Threshold vs Temperature

Figure 4. Enable Threshold vs Temperature

Figure 5 Output Rising Time vs Temperature

Figure 6. Output Falling Time vs Temperature

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FUNCTIONAL BLOCK DIAGRAM

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OPERATION

Overview

The SCT52240A is a dual-channel non-invertible high-speed low side driver with supporting up to 28V wide supply for both power MOSFET and IGBT. Each channel can source and sink 4A peak current along with the minimum propagation delay 13ns from input to output. The 1ns delay matching and the stackable output characteristics support higher driving capability demanding in high power converter application. The ability to handle -

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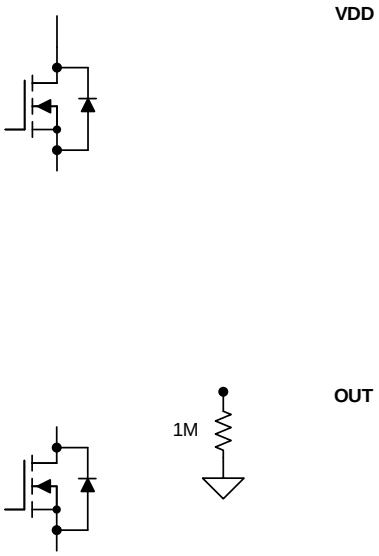

Figure 12. SCT52240A Output Stage

Stackable Output

The SCT52240A features 1ns (typical) delay matching between dual channels, which enables dual channel outputs be stackable when the driven power device required higher driving capability. For example, in a Boost Power Factor Correction converter, there are 2 power MOSFET in parallel to support higher power output capability. The two power MOSFET are preferred to be driven by a common gate control signal. By using SCT52240A, the OUTA and OUTB can be connected together to provide the higher driving capability, so does the INA and INB. As a result, a single input signal controls the stacked output combination. To support the stackable output, each channel output stage artificially implements up to 5ns dead-time to avoid the possible shoot-through between two channels as shown Figure 13.

Due to the rising and falling threshold mismatch between INA and INB, cautions must be taken when implementing stackable output of OUTA and OUTB together. The maximum mismatch between INA and INB input threshold is up to 10mV (maximum cross temperature), as a result the allowed minimum slew rate of input logic signal is 2V/us. The following suggestions are recommended when INA and INB connected together and along with the OUTA and OUTB:

1. Apply the fast slew rate dv/dt on input (2 V/us or greater) to avoid the possible shoot-through between OUTA and OUTB output stage.
2. INA and INB must be connected as close to the pins as possible.

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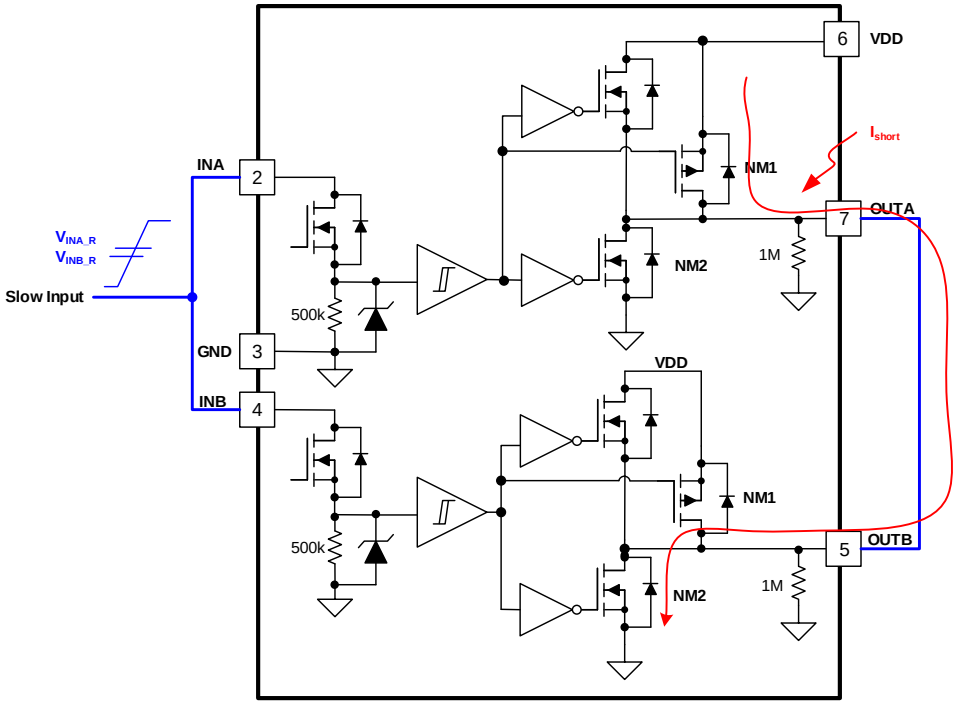

Figure 13. SCT52240A Stackable output

The Figure 14 and Figure 15 shows the stackable output with 2V/us input signal.

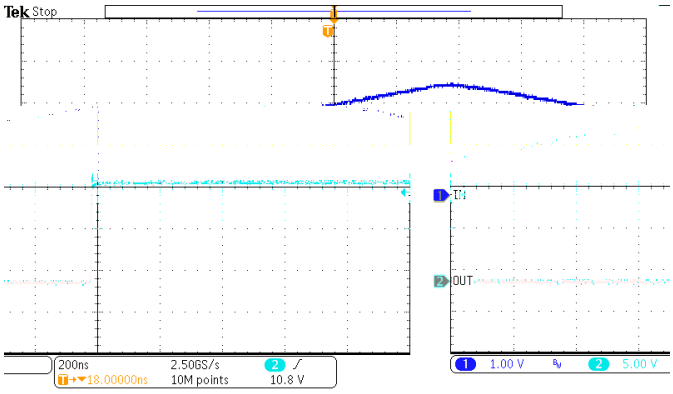

Figure 14. Driver Switching ON

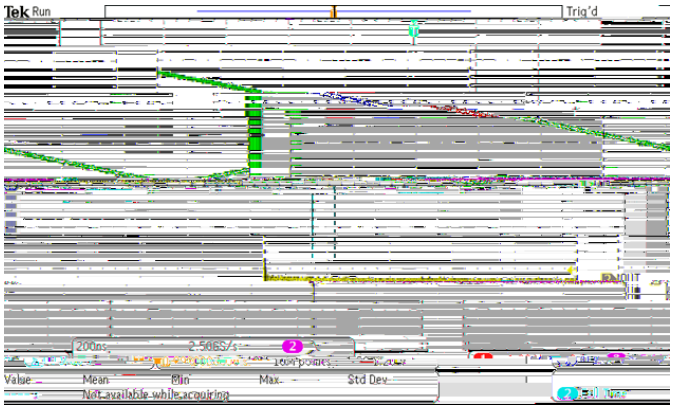

Figure 15. Driver Switching OFF

Thermal Shutdown

Once the junction temperature in the SCT52240A exceeds 170 C, the thermal sensing circuit stops switching until the junction temperature falling below 145 C, and the device restarts. Thermal shutdown prevents the damage on device during excessive heat and power dissipation condition.

APPLICATION INFORMATION

Typical Application

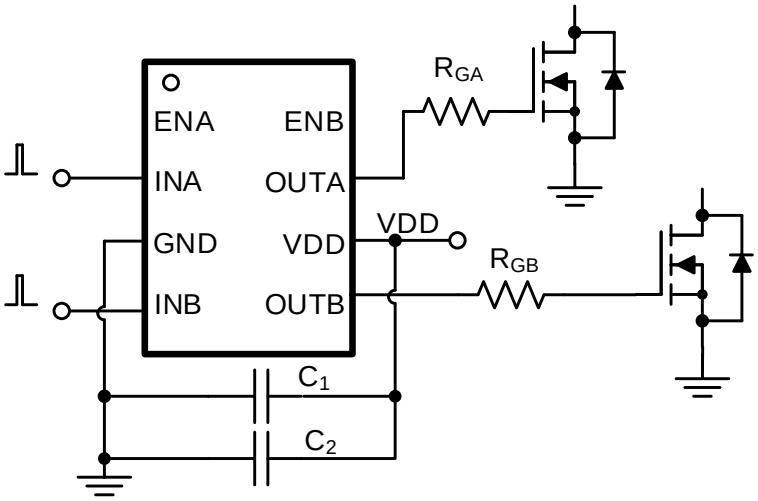

Figure 16. Dual Channel Driver Typical Application

Driver Power Dissipation

Generally, the power dissipated in the SCT52240A depends on the gate charge required of the power device (Qg), switching frequency, and use of external gate resistors. The SCT52240A features very low quiescent currents and internal logic to eliminate any shoot-through in the output driver stage, their effect on the power dissipation within the gate driver is negligible.

For the pure capacitive load, the power loss of each channel in SCT52240A is:

(1)

Where

- V_{DD} is supply voltage
-

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Where

- R_{OH} is the equivalent pull up resistance of SCT52240A
- R_{OL} is the pull down resistance of SCT52240A
- R_G is the gate resistance between driver output and gate of power device.

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Layout Guideline

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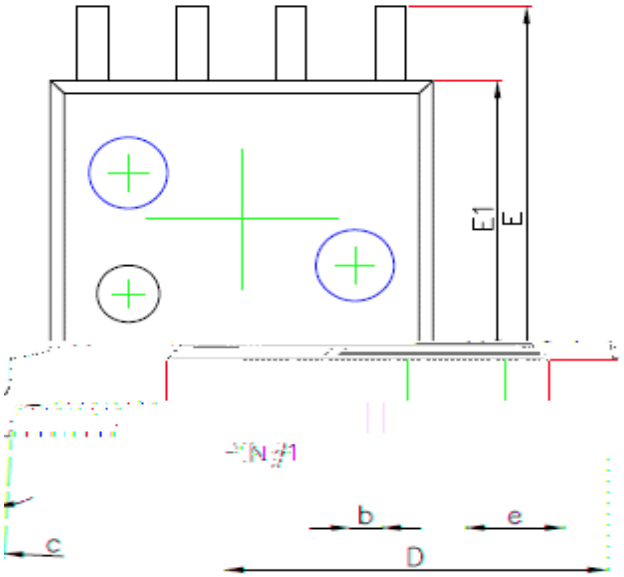
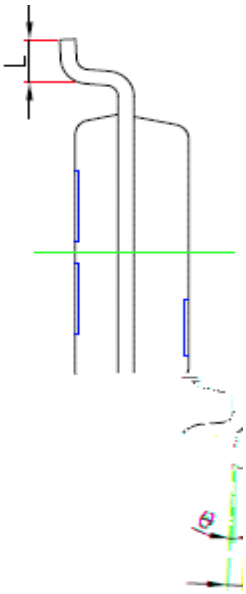
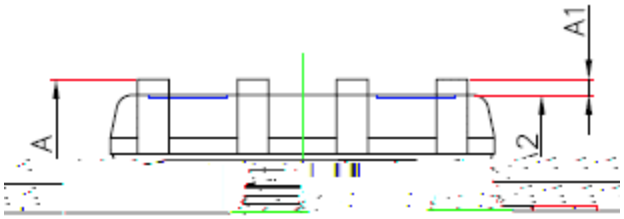
PACKAGE INFORMATION (SOP-8)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	Unit: Millimeter		
	MIN	TYP	MAX
A	1.45	---	1.75
A1	0.1	---	0.25
A2	1.35	---	1.55
b	0.33	---	0.51
c	0.17	---	0.25
D	4.7		5.1
E	5.8		6.2
E1			

NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

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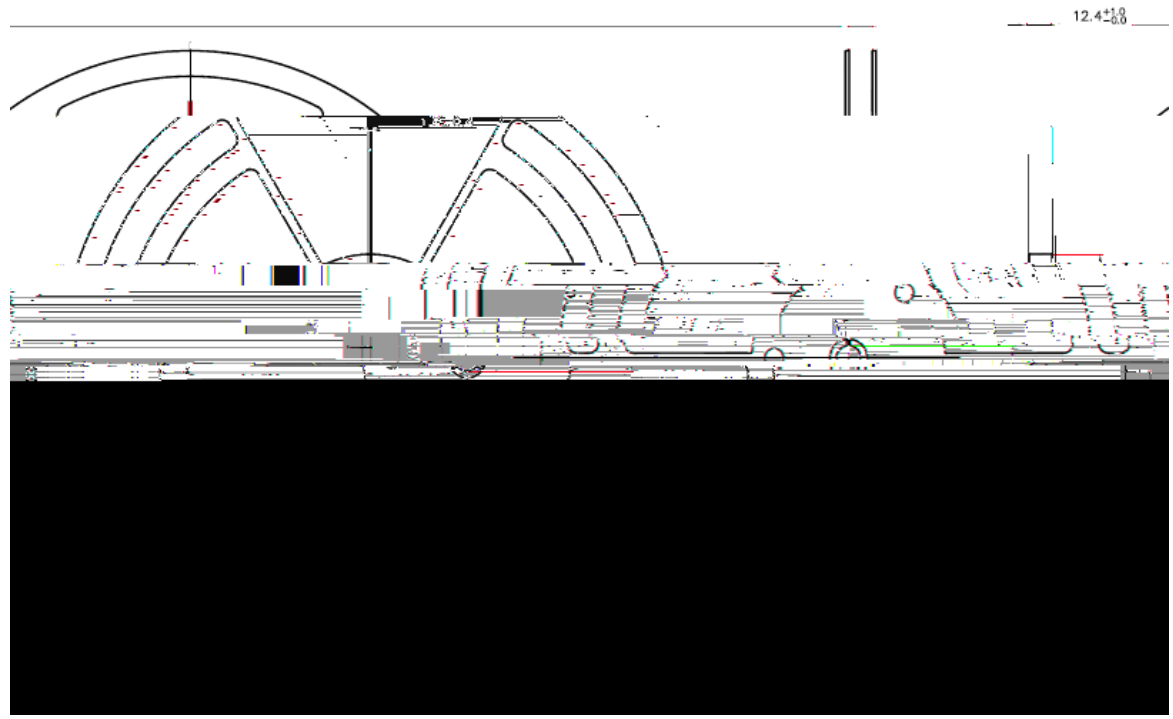
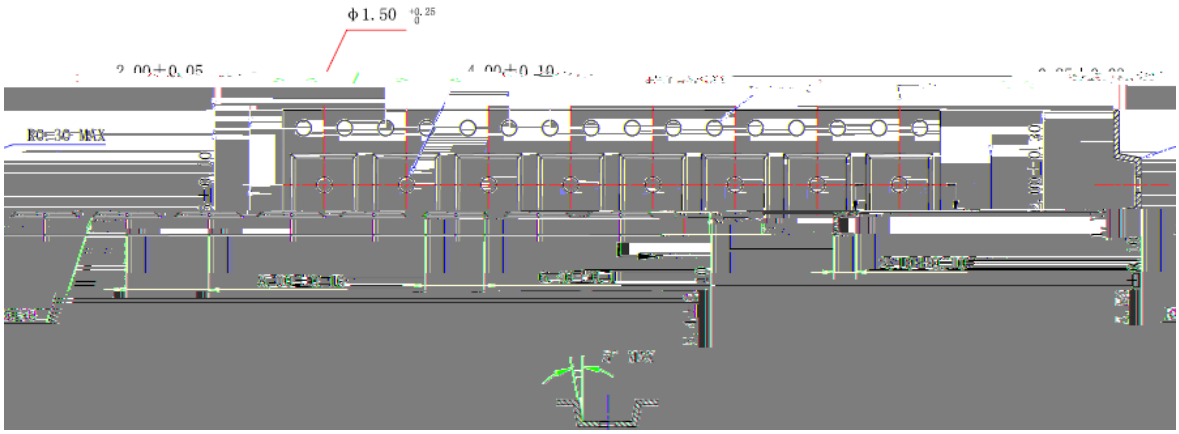
TAPE AND REEL INFORMATION





Feeding Direction

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