Revision 1.0: Released to market

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT44160AMZER	Tape & Reel	4000	160A	28	ETSSOP-28L	3
SCT44160BMZER	Tape & Reel	4000	160B	28	ETSSOP-28L	3
SCT44160CMZER	Tape & Reel	4000	160C	28	ETSSOP-28L	3

Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VS (t < 400 mS)	-0.3	45	V
Reverse polarity voltage	-36		V
Current on GND (t < 2 minutes)	-100	250	mA
Voltage on INx, DIAG_EN, SEL, SEH, and THER	-0.3	7	V
Current on INx, DIAG_EN, SEL, SEH, and THER	-10		mA
Voltage on STx or FAULT	-0.3	7	V
Current on STx or FAULT	-30	10	mA
Voltage on CS	--2.7	7	V
Current on CS		30	mA
Voltage on CL, CL1, CL2, CL3, CL4	-0.3	7	V
Current on CL, CL1, CL2, CL3, CL4		6	mA
Inductive load switch-off energy dissipation, single pulse, single channel		40	mJ
Junction temperature(2)	-40	150	C
Storage temperature T_{STG}	-65	150	C

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PARAMETER	THERMAL METRIC	ETSSOP-28L	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	24.27	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	32.11	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	2.49	
$R_{\theta JB}$	Junction to board thermal resistance(1)	9.17	
$R_{\psi JT}$	Junction-to-top characterization parameter	2.96	

(1) SCT provides R_{θ}

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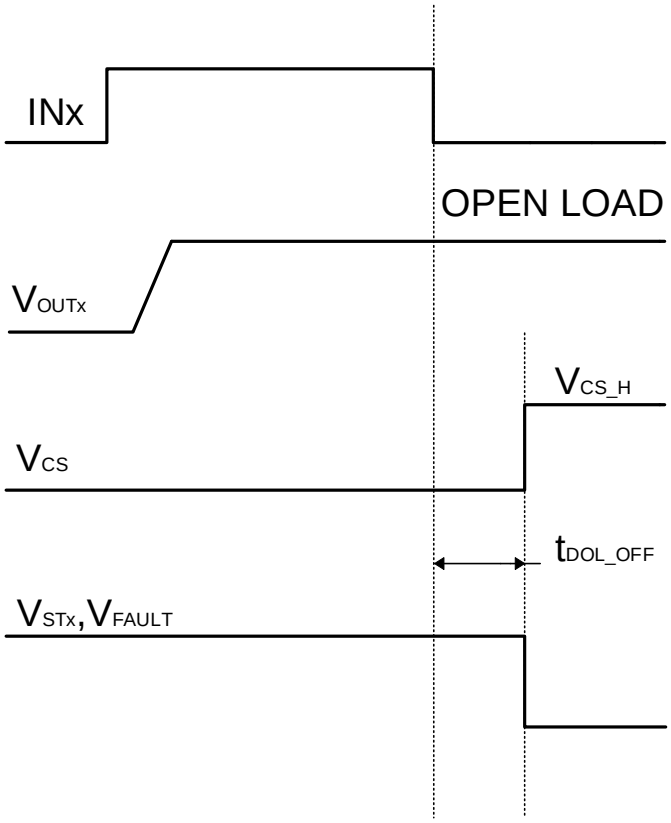
Logic Input(INx,DIAG_EN,THER,SEH,SEL)					
V_{IH}	Logic high-level voltage		1.35	1.55	V
V_{IL}	Logic low-level voltage				

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I_{CS_H}	Current-sense pin output current	V_{CS} =4.5V	10	22		mA
I_{CS_LKG}	Current-sense leakage current in disabled mode	DIAG_EN=0V,TJ=125			0.5	uA
Switching						
t_{D_ON}	Input to output propagation delay, Rising	DIAG_EN=5V, I_{OUTx} =0.5A, INx rising edge to 10% of V_{OUTx}		30		uS
t_{D_OFF}	Input to output propagation delay, Falling	DIAG_EN=5V, I_{OUTx} =0.5A, INx falling edge to 90% of V_{OUTx}		8		uS
V/ $t_{_ON}$	Turnon slew rate	DIAG_EN=5V, I_{OUTx} =0.5A, V_{OUTx} from 10% to 90%		0.35		V/uS
V/ $t_{_OFF}$	Turnoff slew rate	DIAG_EN=5V, I_{OUTx} =0.5A, V_{OUTx} from 90% to 100%		0.4		V/uS
t_{D_MATCH}	t_{D_RISE} - t_{D_FALL}			20		uS
Current Sense timing						
$t_{CS_ON(EN)}$	CS settling time from DIAG_EN disabled	I_{OUTx} =0.5A, DIAG_EN rising edge to V_{CS} rising		3	10	uS
$t_{CS_OFF(EN)}$	CS settling time from DIAG_EN enabled	I_{OUTx} =0.5A, DIAG_EN falling edge to V_{CS} falling		2	10	uS
$t_{CS_ON(IN)}$	CS settling time from IN rising edge	DIAG_EN=5V, I_{OUTx} =0.5A, INx rising edge to V_{CS} rising		100	160	uS
$t_{CS_OFF(IN)}$	CS settling time from IN falling edge	DIAG_EN=5V, I_{OUTx} =0.5A, INx rising edge to V_{CS} rising		3	10	uS
t_{SEx}	Multi-sense transition delay from channel to channel	DIAG_EN=5V,Current sense output delay when multi-sense pins SEL and SEH transition from channel to channel		100		uS

Figure 1. Output And CS Delay Sequential

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Figure

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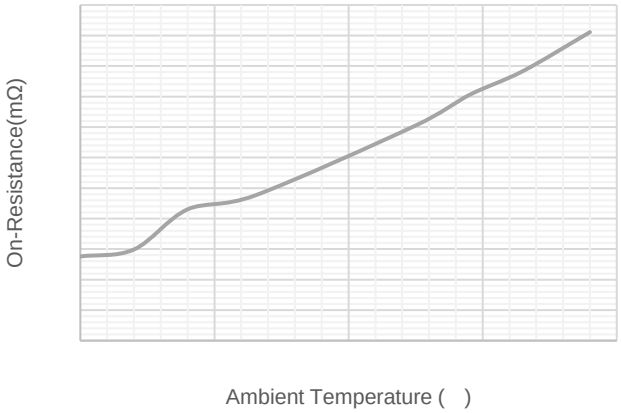


Figure 10. Channel-3 FET On-Resistance VS Temperature

Figure 11. Channel-4 FET On-Resistance VS Temperature

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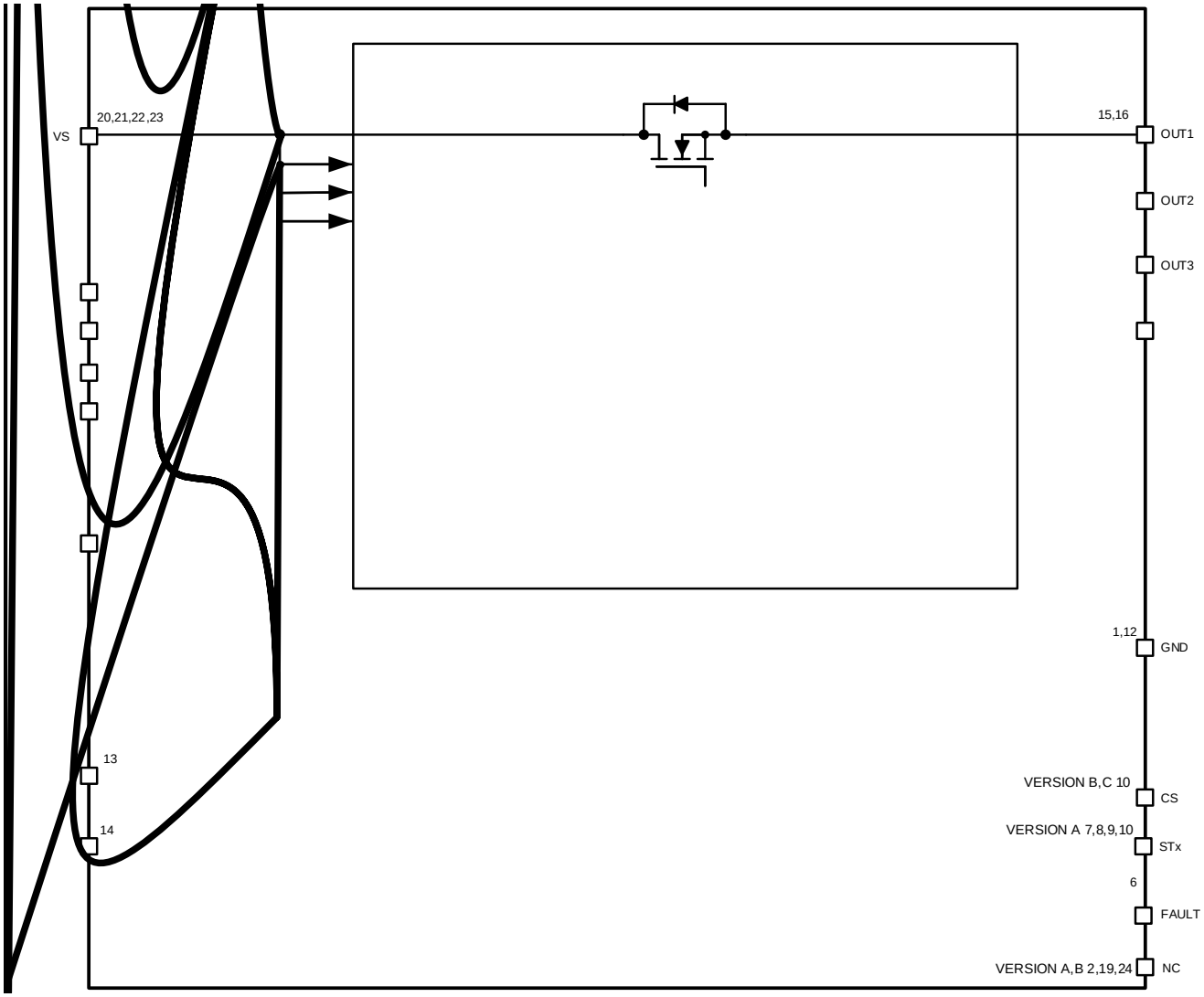


Figure 12. Functional Block Diagram

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Overview

SCT44160 is a four-channel intelligent high-side switch that internally integrates a charge pump and four power N-MOSFETs. SCT44160 offers external adjustable threshold overcurrent protection functionality, with a typical value of 7A for internal current limiting to enhance design flexibility and system reliability. This device features comprehensive diagnostic functions and high-precision current sensing functions to achieve smart control of the load. Among SCT44160's three versions, Version A includes an open-drain digital output diagnostic mode. Version B provides current sensing analog output. Version C provides four external adjustment functions for overcurrent thresholds based on version B.

In Version A, an open-drain digital output is utilized, and the diagnostic output pin STx needs to be pulled down to the ground externally by providing a pull-up voltage of 3.3V or 5V to match the MCU. The abnormal status of each channel in version A can be reported separately to help the system quickly locate problematic channels.

Version B has a current sensing analog output, enabling the system to accurately determine the operational status of each channel. The integrated current mirror of the device provides a mirror current of $1/K_{CS}$ load current, which flows through the CS resistor and becomes a voltage signal to achieve analog output of load current. Version B can achieve the current information detection function for each channel through cyclic selection of SEH SEL pins. Additionally, in the event of an abnormality in a specific channel, the global diagnostic function of the Fault pin can be employed to pinpoint the problematic channel.

The diagnostic function of version C is consistent with version B, but version C can set four overcurrent thresholds separately. Four overcurrent thresholds can be reasonably set according to the application environment, further improving the flexibility and reliability of system design.

SCT44160 has a clamping function between the drain and source electrodes, which can effectively protect itself under inductive load conditions.

SCT44160 is an intelligent high-side switch suitable for applications where resistance, capacitance, and inductance loads can support most small load currents.

Adjustable Current Limit

SCT44160 has an adjustable high-precision current limitation mechanism. When the load current reaches the designated threshold, it rapidly internally controls the N-MOSFET gate voltage to clamp the output current to the set value and report faults. When overcurrent occurs, there is high power dissipation in the device. If the device heats up and triggers thermal shutdown, the current limit will be reduced to $I_{CL\ (TSD)}$ to reduce power dissipation on the device and further protect the device.

SCT44160 has two overcurrent protection thresholds, internal and external.

Internal current limitation, SCT44160 has a conventional value of 7A for internal integrated current limitation. When

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Accurate Current Sense

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SEL pins for multi-channel current detection and fault report multiplexing, and select the corresponding channel of the CS pin to read whether the voltage of the CS pin is V

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IC GND and the DIAG_EN or THER pin connected to external ground. Regardless of whether INx is high or low, the channels will be deactivated for protection.

Thermal Shutdown

Under extreme conditions like overcurrent, the device undergoes substantial power stress and heats up rapidly. SCT44160 incorporates two types of thermal protection: absolute thermal protection and relative thermal protection. These are designed to prevent rapid overheating of the device without protection.

When absolute overheating occurs, the thermal shutdown will be triggered, and the behavior after thermal shutdown can be determined by configuring THER:

1.

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MCU I/O Protection

In some extreme cases, such as inductive load input disconnection, negative voltage pulses may appear in the IC

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Typical Application

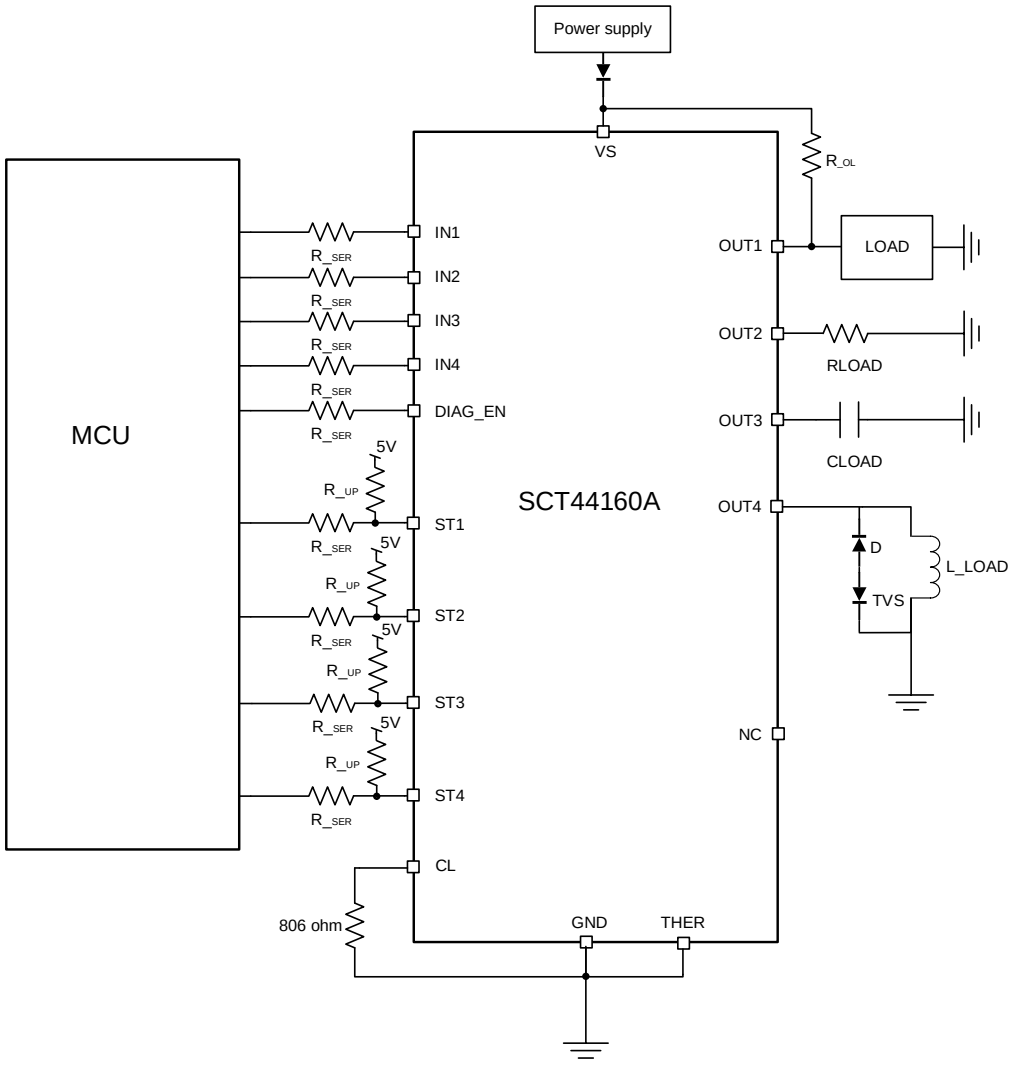


Figure 19. Version A Application Schematic

Design Parameters

Design Parameters

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Typical Application (continued)

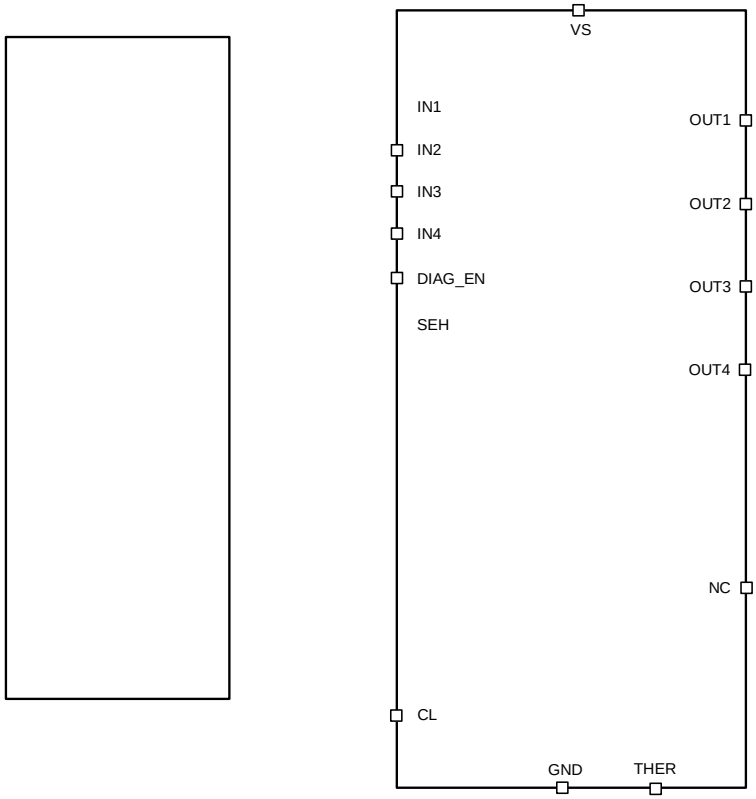


Figure 20. Version B Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	13.5V Normal 8V to 18V
Load Current	Typical 1A
Current Limit	2.5A

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Typical Application (continued)

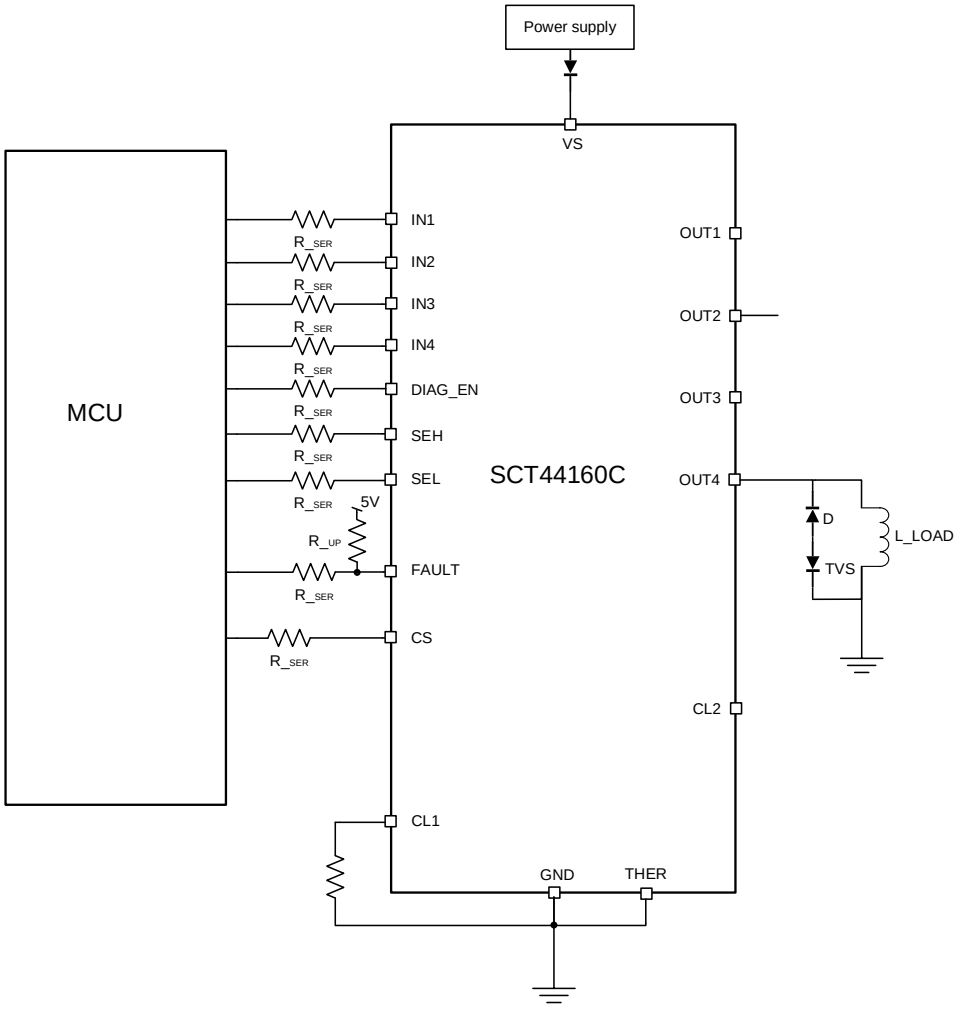


Figure 21. Version C Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	13.5V Normal 8V

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Application Waveforms

V_{VS}=13.5V, unless otherwise noted

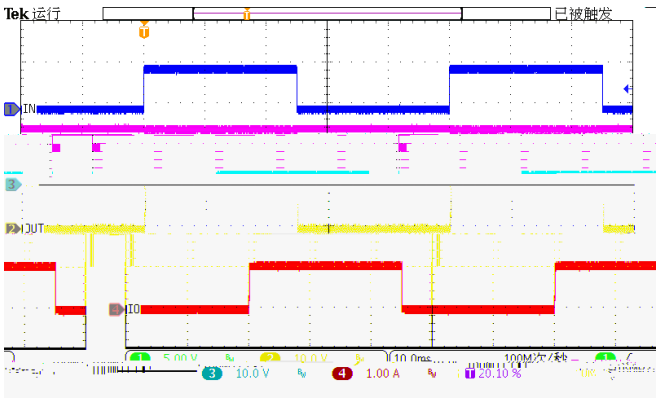


Figure 22. IN Toggle resistive load 1A

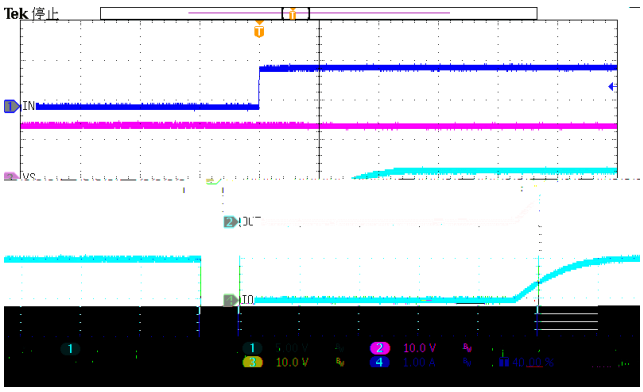


Figure 23. IN On resistive load 1A

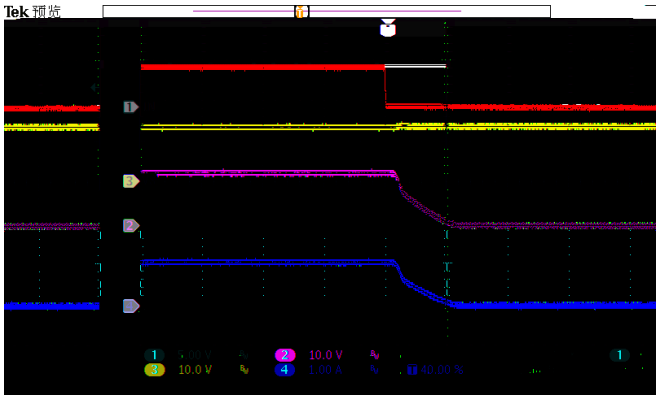


Figure 24. IN Off resistive load 1A

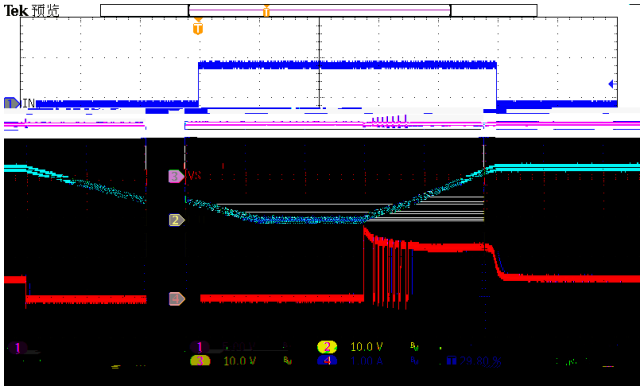


Figure 25. IN Toggle capacitive load C=2.2mF

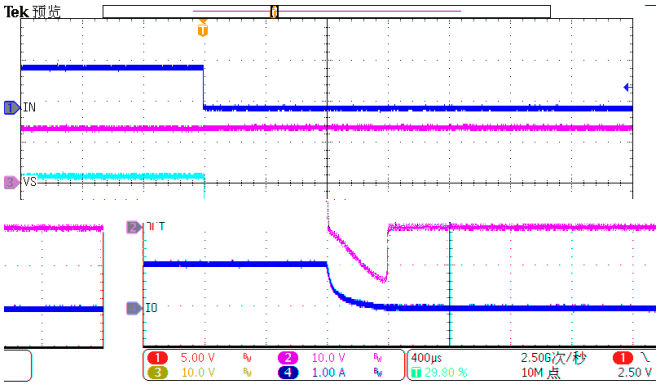


Figure 26. IN Off Inductive load L=8mH series resistor=13.5Ω

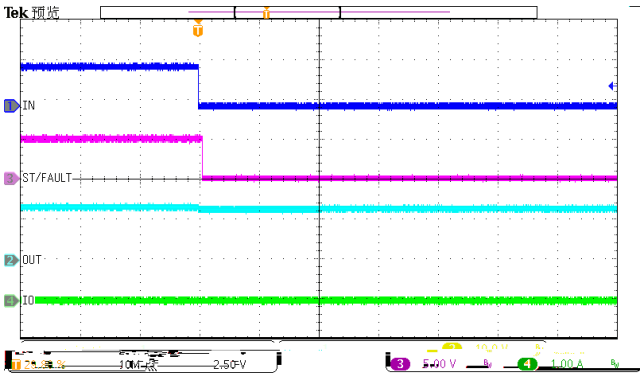


Figure 27. Open-load detection

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Application Waveforms(continued)

V_{VS}=13.5V, unless otherwise noted

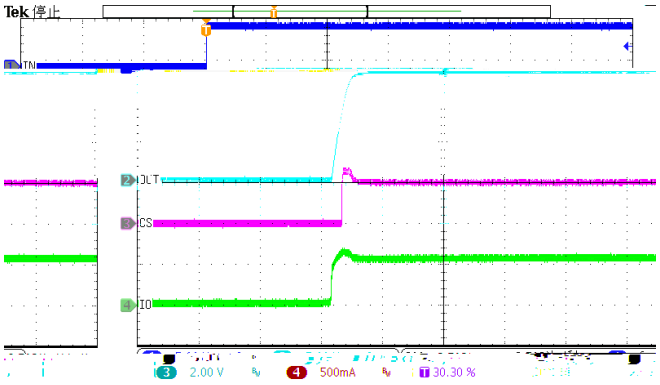


Figure 28. IN On current sense load=0.5A

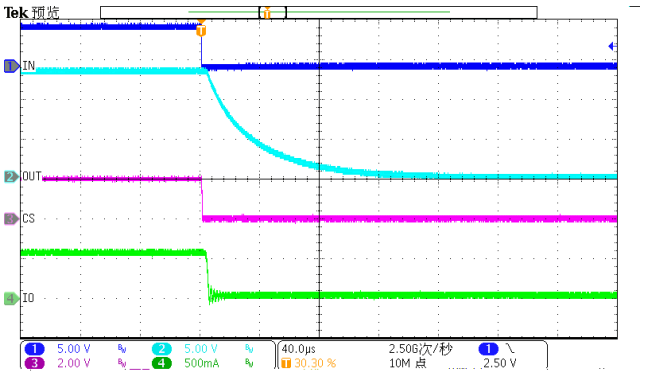


Figure 29. IN Off current sense load=0.5A

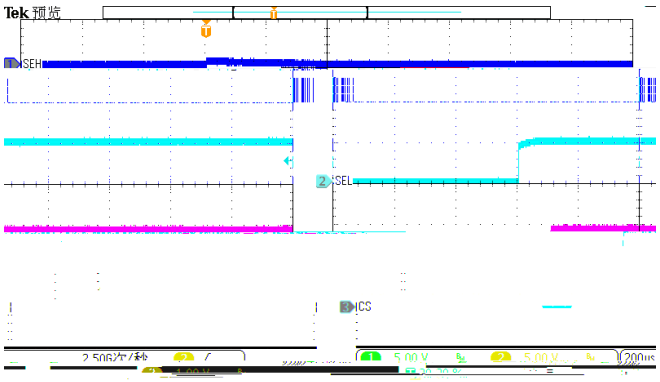


Figure 30. Current sense CH1-CH2

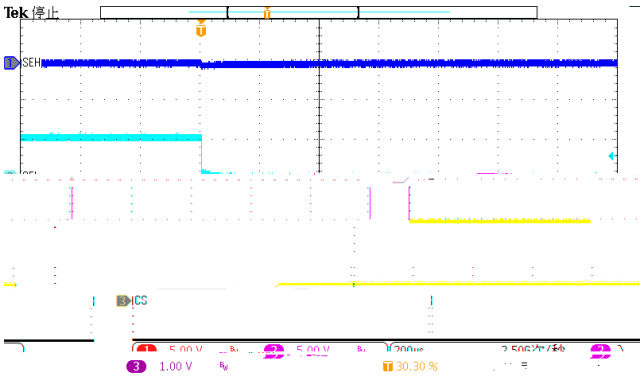


Figure 31. Current sense CH2-CH1

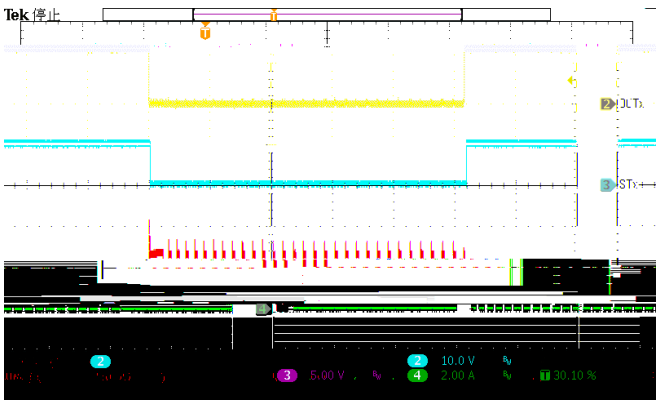


Figure 32. Overcurrent detection for version A

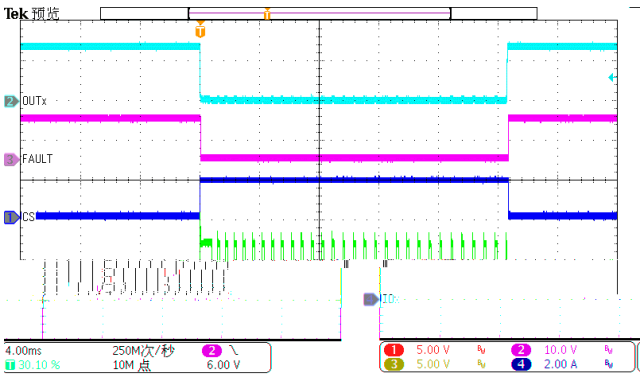


Figure 33. Overcurrent detection for version B/C

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Layout Guideline

The PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

1. Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
2. More vias should be placed below the device Thermal PAD to further improve heat transfer.
3. R_{CL} should be connected to IC GND.

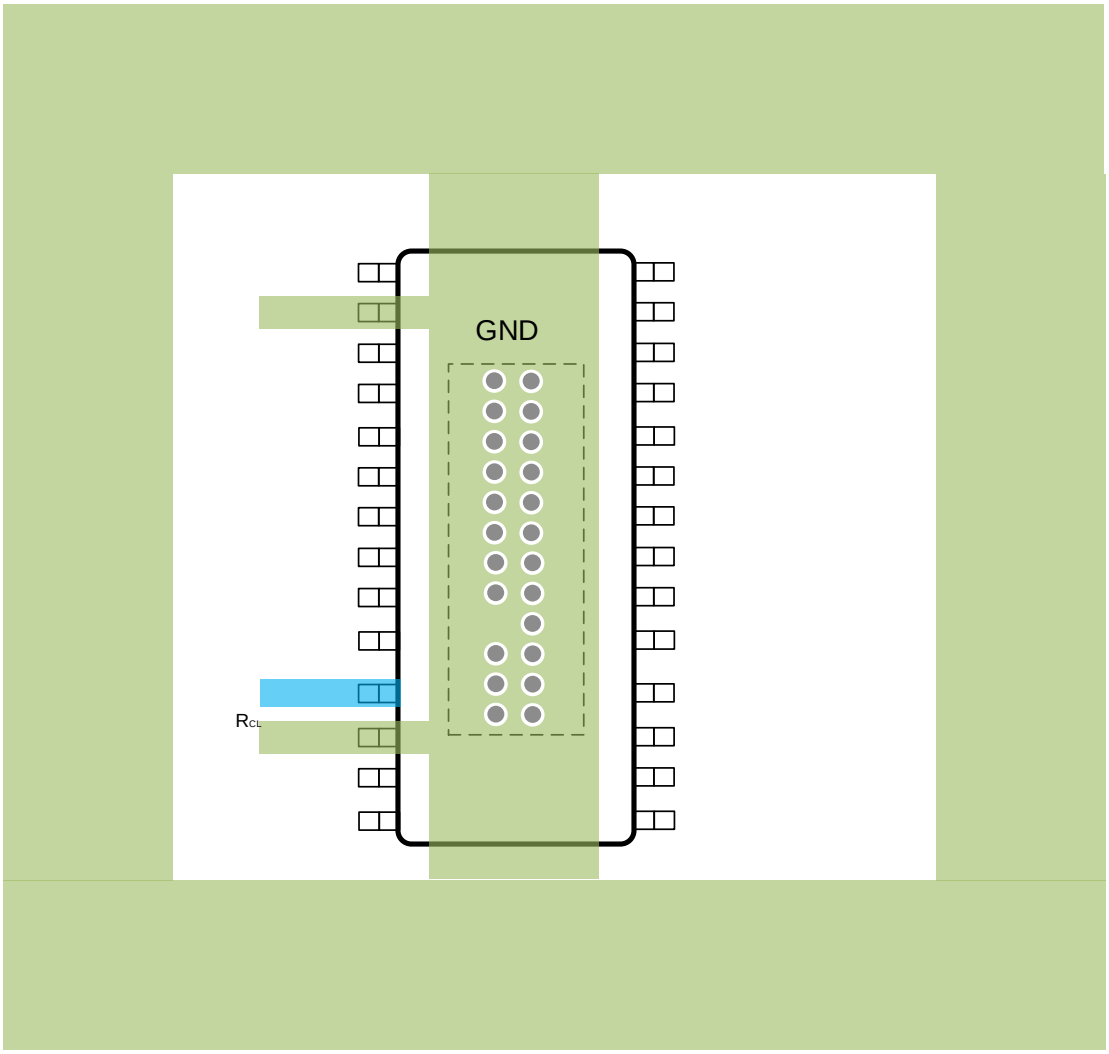


Figure 34. Without a GND Network PCB Layout

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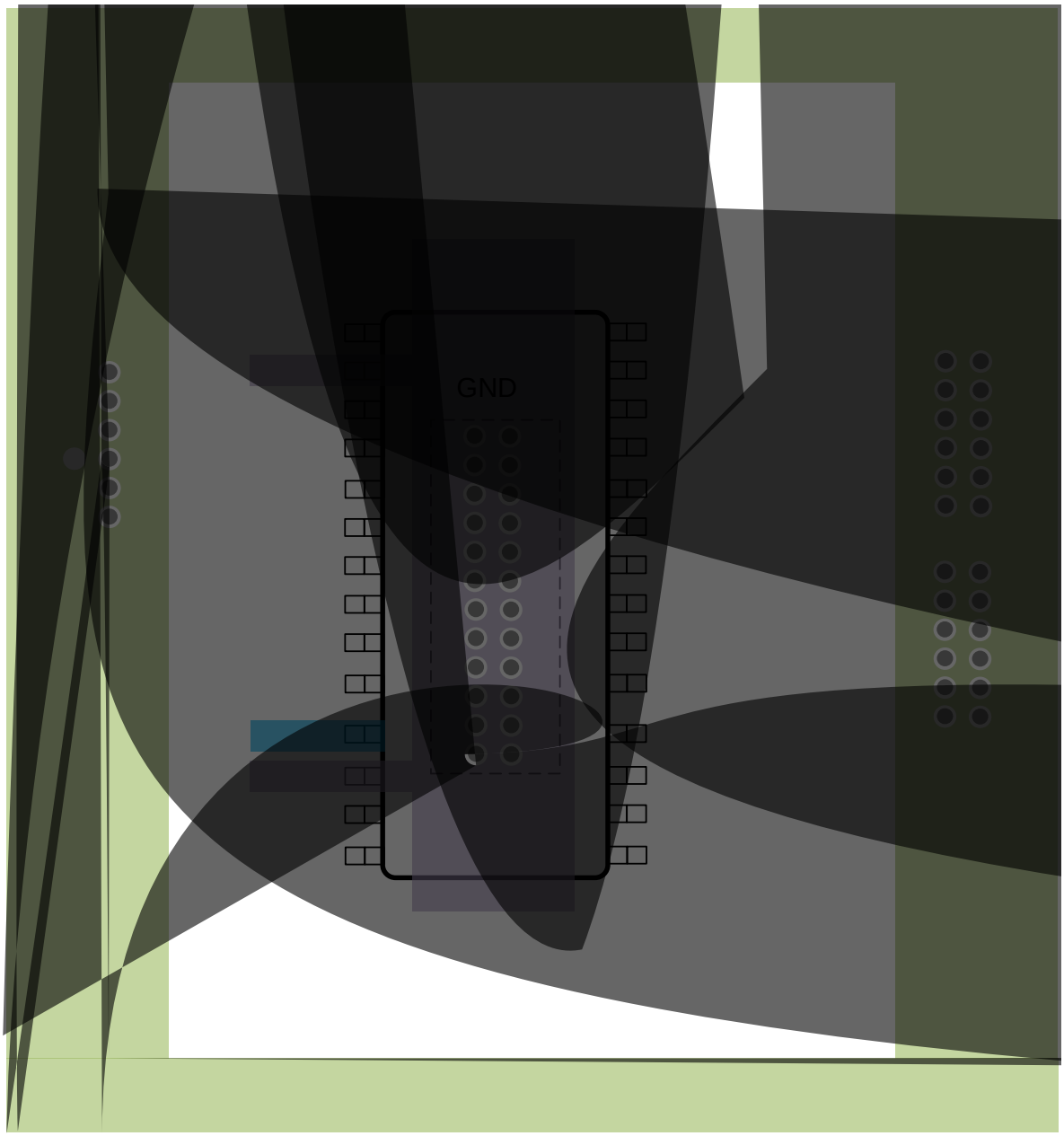
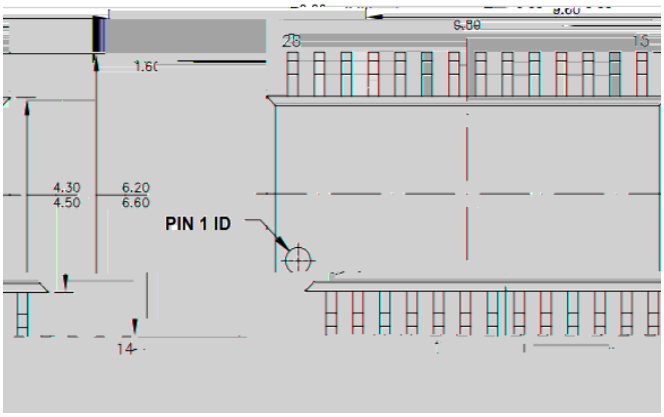
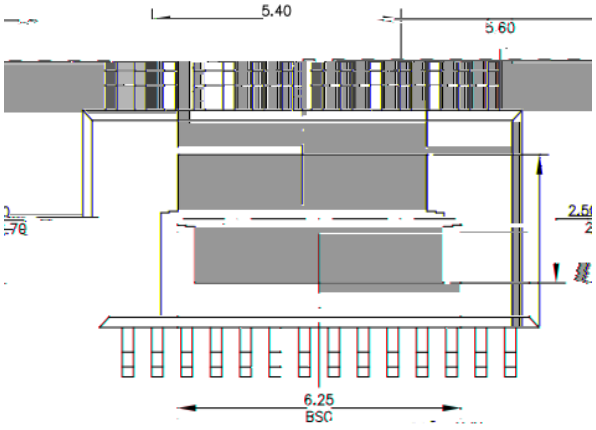


Figure 35. With a GND Network PCB Layout

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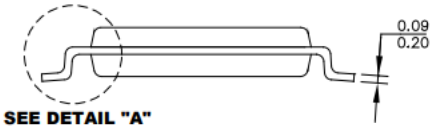
TOP VIEW



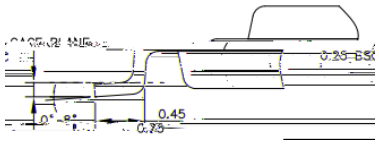
BOTTOM VIEW



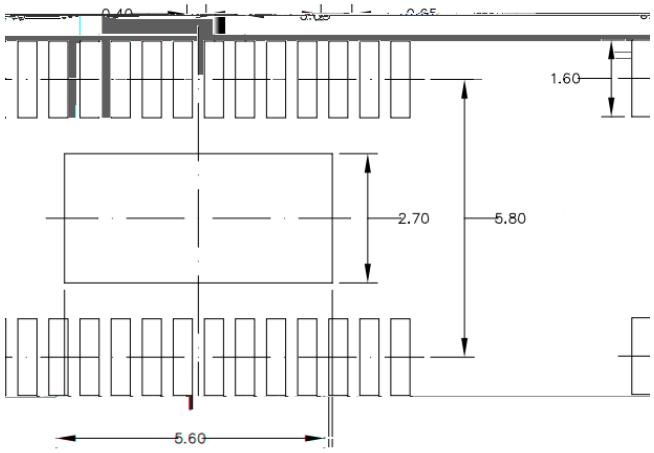
FRONT VIEW



SIDE VIEW



DETAIL "A"

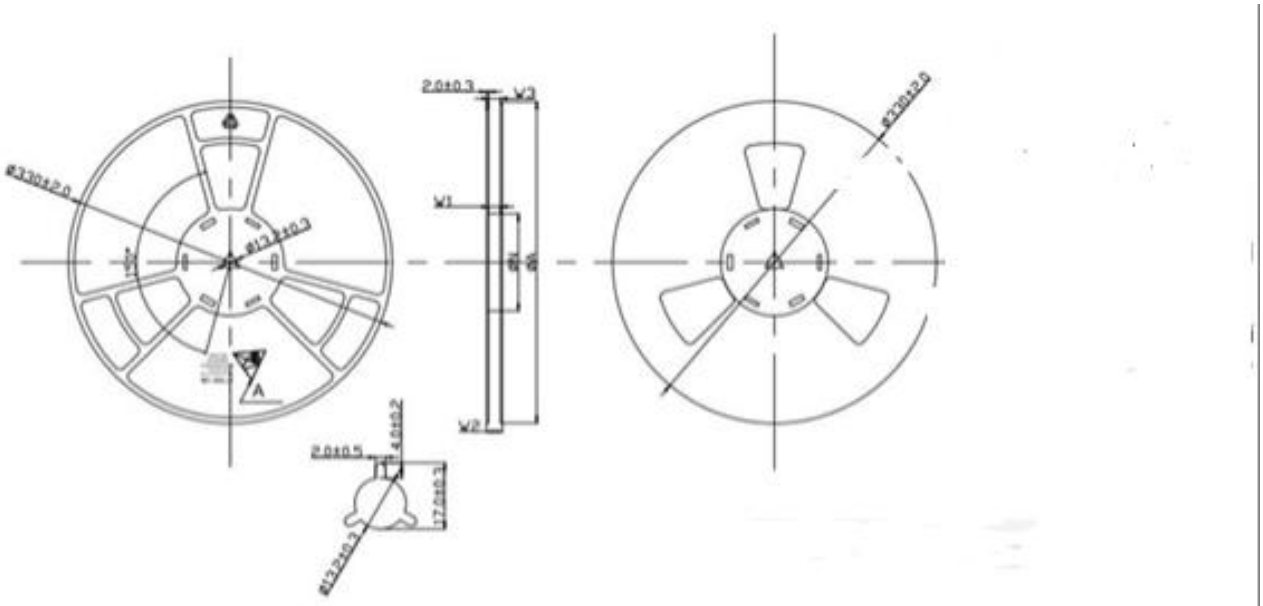


RECOMMENDED LAND PATTERN

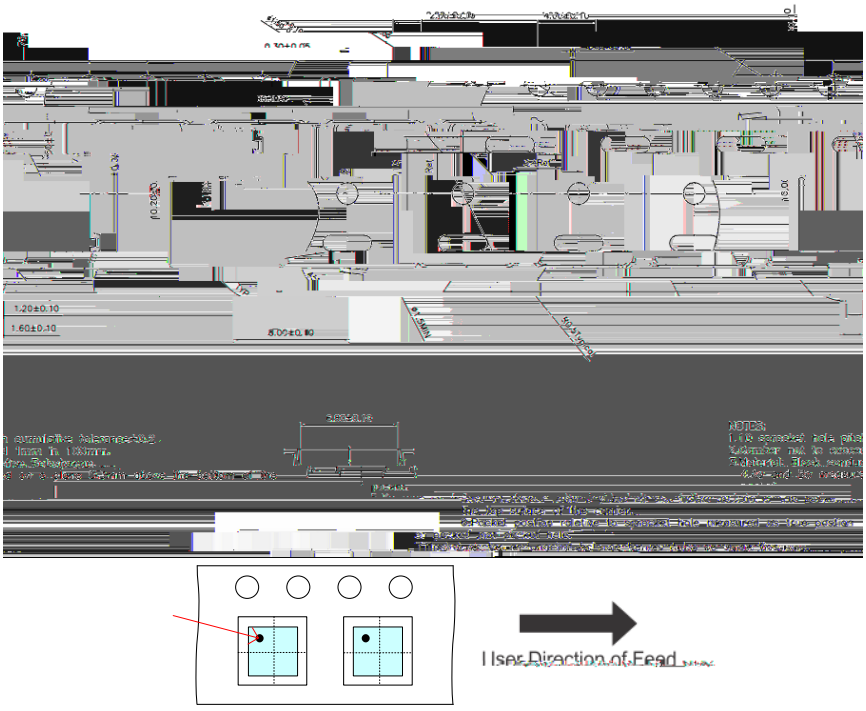
NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS..
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3. PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6. DRAWING IS NOT TO SCALE.

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PRODUCT SPECIFICATIONS					
TYPE WIDTH	ØA	ØN	W1	W2(Max)	W3(Min)
16MM	330±2.0	100±1.0	16.4	22.4	15.9/19.4



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