NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to production.

Revision 1.1: Update the Figure 8 and Figure 26 and R

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R evision 1⁄ U pdatU

9	Thermal Pad	Connect the thermal pad to a large area GND plane for improved thermal performance.

Over operating free-air temperature range unless otherwise noted

V_{IN}	Input voltage range	2.2	5.5	V
V_{OUT}	Output voltage range	0.8	5	V
V_{EN}	Enable input voltage	0	V_{IN}	V
C_{IN}	Input capacitor	2.2	--	uF
C_{OUT}	Output capacitor	2.2	220	uF
ESR	Output capacitor ESR requirements	0.001	5	q
T_J	Operating junction temperature	-40	125	°C

Over operating free-air temperature range unless otherwise noted (1)

V_{IN}	Maximum input voltage range	-0.3	6	V
V_{OUT}	Maximum output voltage range	-0.3	6	V
V_{EN}	Maximum enable input voltage	-0.3	V_{IN}	V
T_J (2)	Junction temperature range	-40	150	°C
T_{stg}	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 150°C

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The value of $R_{\theta JA}$ and $R_{\theta JC}$ given in this table is only valid for compario

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$V_{IN}=V_{OUT}+1V$, $C_{OUT}=10uF$, T_J= -40°C~125°C, typical value is tested under 25°C.

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I_{EN_0V}	Enable pin current	EN=0			0.2	εA
$I_{EN\_3.3V}$	Enable pin current	EN=3.3V		0.01	0.2	εA
$R_{EN\_pulldown}$	enable pulldown resistor			648		kq
T_{SS}	Soft-start time		0.5	2.4	4.5	ms

V_{PG_R}	PG rising threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} rising		88%		
V_{PG_F}	PG falling threshold percentage	$V_{OUT}/V_{OUT(NOM)}$,when V_{OUT} falling		82%		
V_{PG_LOW}	PG output low voltage	PG sink 0.5mA		84		mV
R_{PG}	PG pull down resistor	$R_{PG}=V_{PG\_LOW}/0.5mA$		168		q
I_{PG_LKG}	PG leakage current	PG=5V, V_{OUT} in regulation			0.2	uA
$Td_{\_PGR}$	PG signal turn to highe					

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Figure 7. Output Voltage vs Output Current

Figure 8. Shutdown Current vs Ambient Temperature

Figure 9. Output Current Limit vs Ambient Temperature

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Figure 13. PSRR vs Frequency
VIN=4.3V, Cf=33pF,COUT=10uF,IOUT=10mA

Figure 14. PSRR vs Frequency
VIN=3.3V,VOUT=1.2V,Cf=33pF,COUT=10uF

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The SCT71010A00 product are 1A output current linear regulators with very low quiescent current. These voltage regulators operate from 2.2V to 5.5V DC input voltage with supporting 6V transient input voltage an su sep

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The power-good (PG) pin is an open-drain output and can be connected to any 5V or lower rail through an external pull-up resistor. The PG output is high-impedance when VOUT is greater than the PG trip threshold (V_{PG_R}=88% x $V_{OUT(NOM)}$). If VOUT drops below V_{PG_F}=82% x $V_{OUT(NOM)}$, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

The power-good delay time ($Td_{\_PGR}$) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{PG_R}) to when the PG output is high. This power-good delay time is set by an internal time, which is170us typical. The power-

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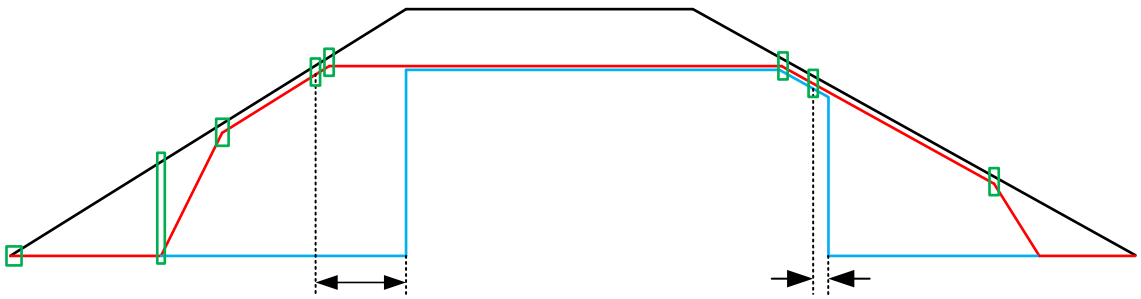

Figure 20. Startup and Shutdown Example —SCT71010 Series

This device incorporates a thermal shutdown (T_{SD}) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the T_{SD} trip point. The junction temperature exceeding the T_{SD} trip point causes the output to turn off. When the junction temperature falls below the T_{SD} trip point minus thermal shutdown hysteresis, the output turns on again.

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backward from the VOUT to the VIN when the VIN shorts to the GND. In order to minimize the damage in such case, use a capacitor with a capacitance less than 220εF. Also by inserting a reverse polarity diode in to the VIN, it can prevent reverse current from reverse battery connection or the case, when the point A is short-circuited GND. If there may be any possible case point B is short-circuited to GND, we also recommend using a bypass diode between the VIN and the VOUT.

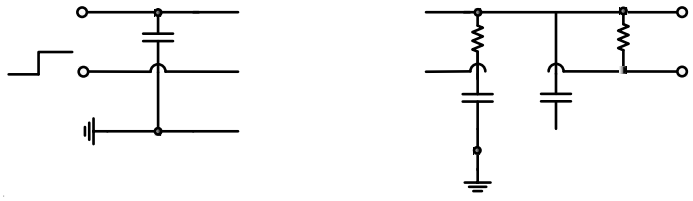

Figure 23. SCT71010A00 Typical Application Schematic with Large Output Capacitor

Input Voltage	5V

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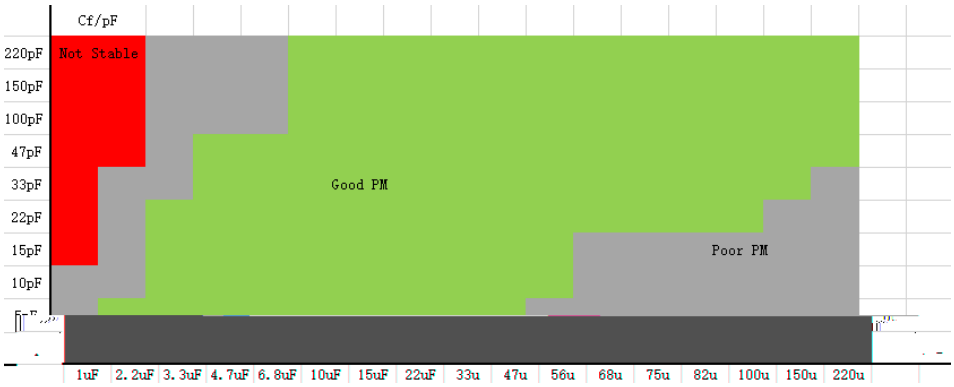

Figure 24. SCT71010A00 Feed Forward Capacitors recommend(R2=100kq ,VOUT=1.8V)

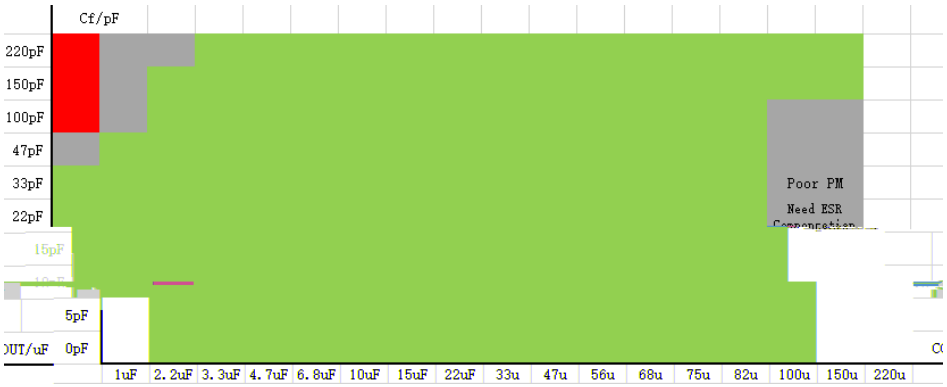

Figure 25. SCT71010A00 Feed Forward Capacitors recommend(R2=10kq ,VOUT=1.8V)

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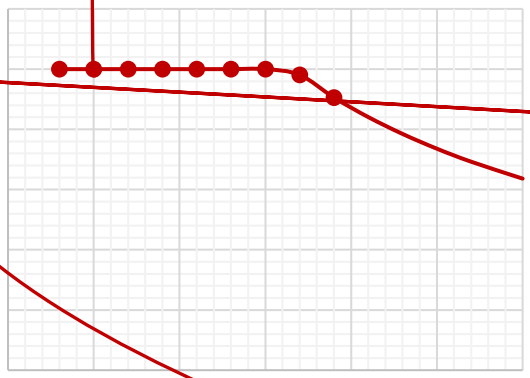

Figure 26. Maximum Output Current vs Input Voltage, VOUT=1.8V of DFN3X3-8L ,$T_J \leq$ TSD_R

Figure 27. Maximum Output Current vs Input Voltage, DFN3X3-8L,TJ ≤ 125

Figure 28. Maximum Allowed Power Dissipation vs Ambient Temperature, DFN3X3-8L,TJ ≤ 125

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Vin=Vout +1V, unless otherwise noted

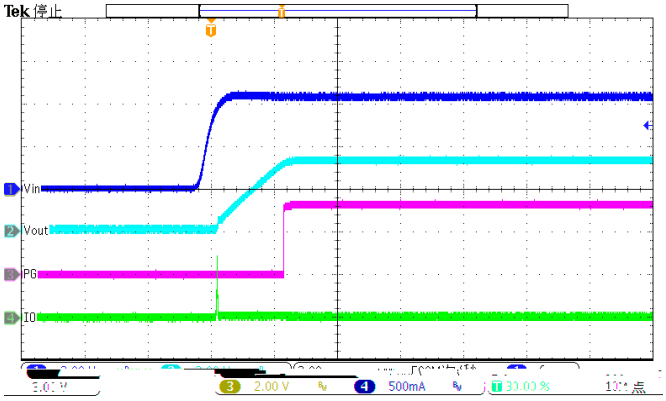

Figure 29. Power up (Iload=10mA)



Figure 30. Power down (Iload=10mA)

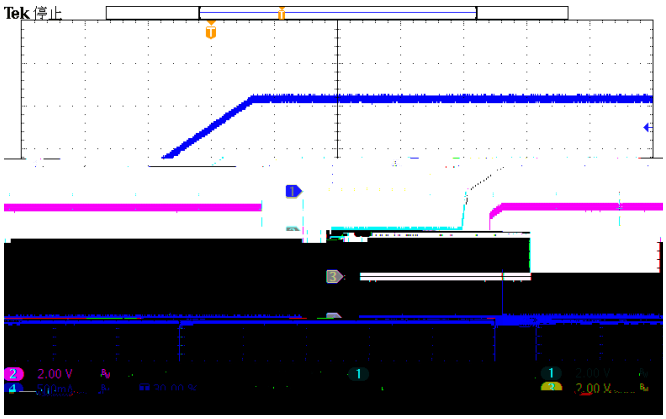

Figure 31. Slow Power up (Iload=10mA)

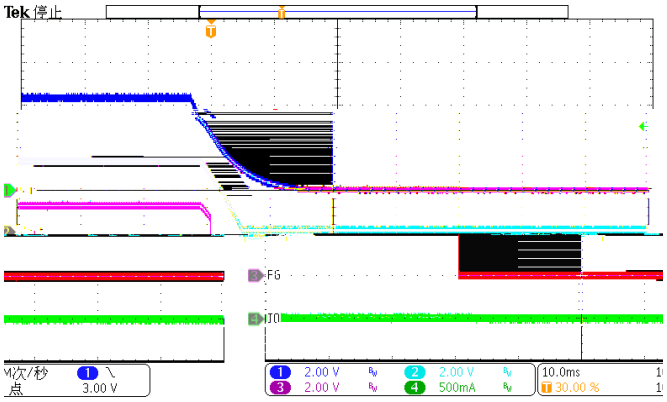

Figure 32. Slow Power down (Iload=10mA)

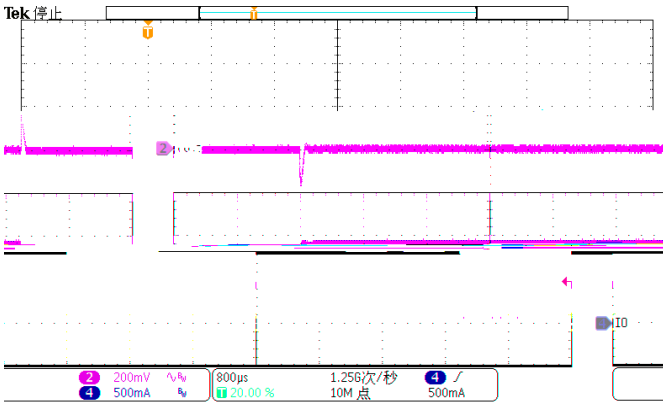

Figure 33. DC-DC Load Transient (100mA-900mA),VOUT=3.3V

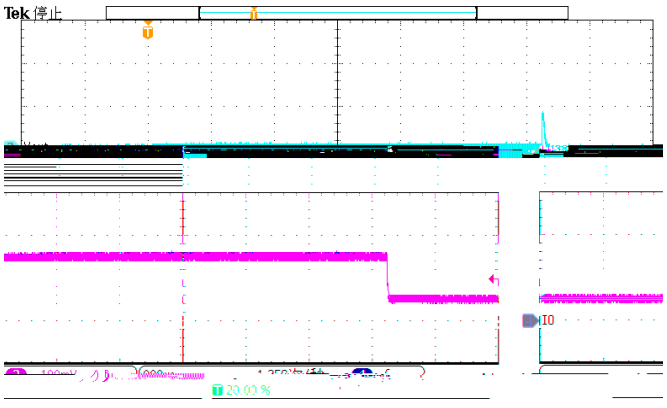

Figure 34. DC-DC Load Transient (250mA-750mA),V_{OUT}=3.3V

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Vin=Vout +1V, unless otherwise noted

Figure 35. Enable (Iload=10mA)

Figure 36. Disable (Iload=10mA)

Figure 37. Enter Short Circuit Protection

Figure 38. Exit Short Circuit Protection

Figure 39

Proper PCB layout is a critical for SCT71010ôs stability, transient performance and good regulation characteristics. For better results, follow these guidelines as below:

1. Both input capacitors and output capacitors must be placed as close to the device pins as possible.
2. It is recommended to bypass the input pin to ground with a 0.1ε F bypass capacitor. The loop area formed by the bypass capacitor connection, V_{IN} pin and the GND pin of the system must be as small as possible.
3. It is recommended to use wide trace lengths or thick copper weight to minimize Iĭ R drop and heat dissipation.
4. To improve the thermal performance of the device, and maximize the current output at high ambient temperature, SCT recommends spreading the copper under the thermal pad as far as possible and al p] / ! Ï

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